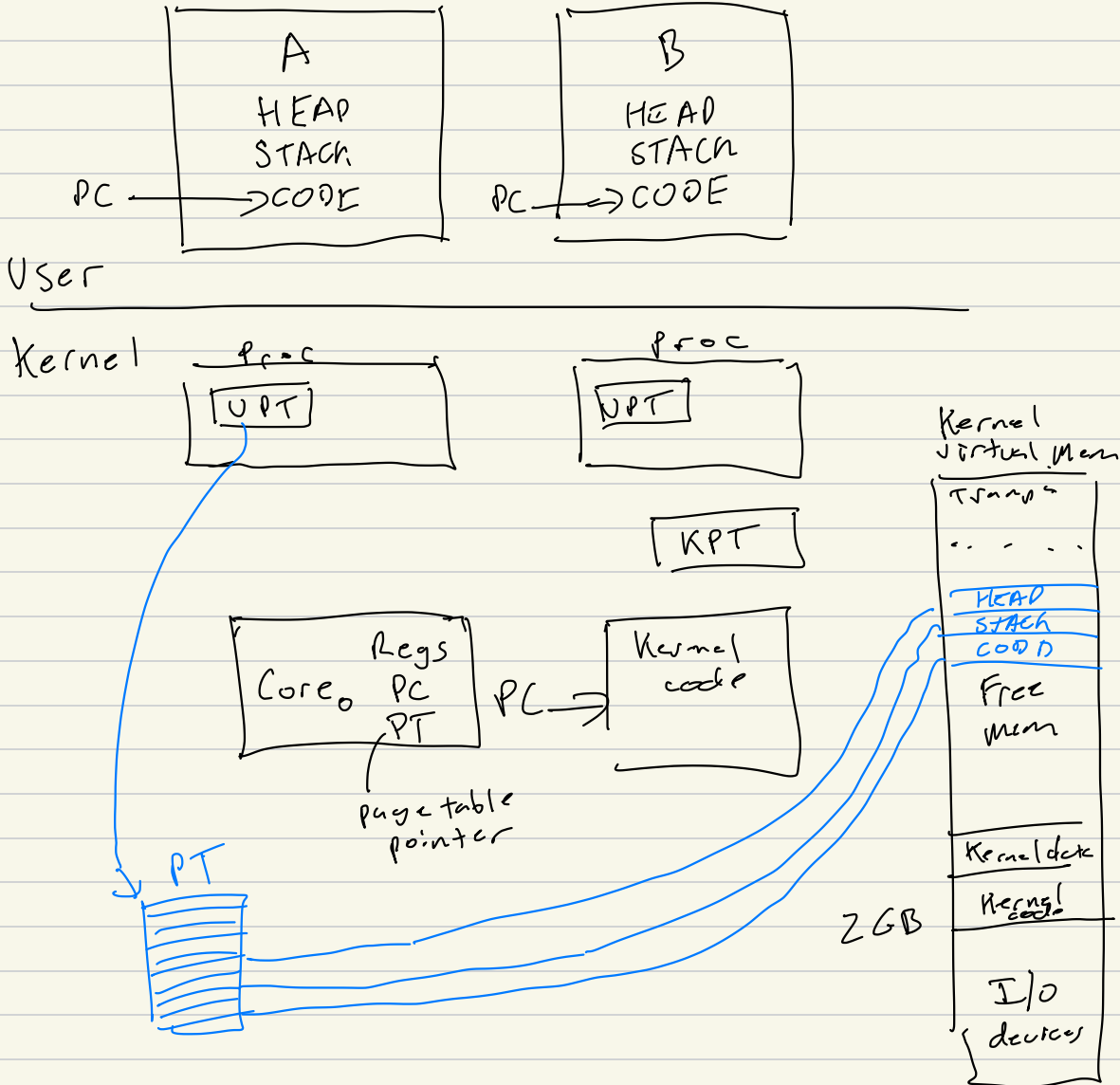


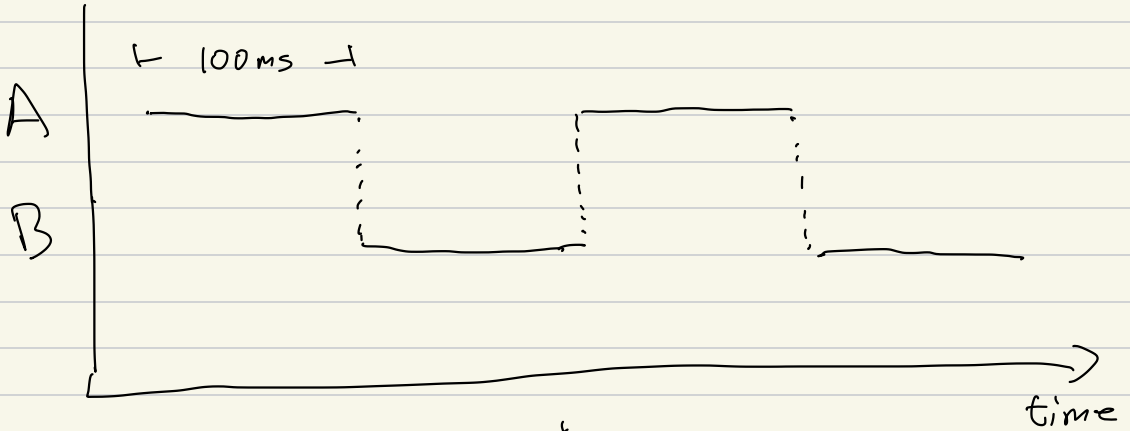
# Process scheduling Page Tables



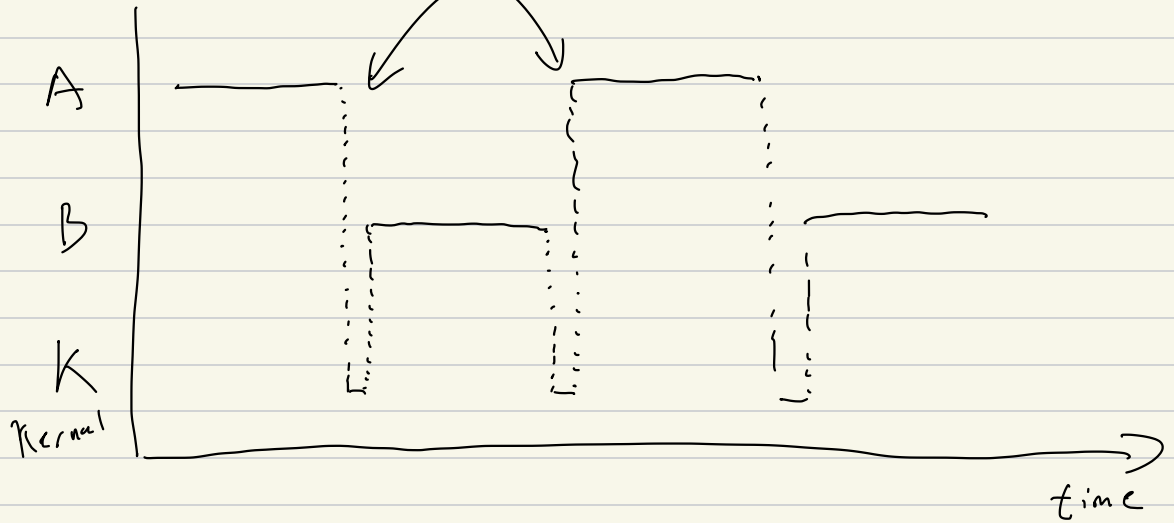
A

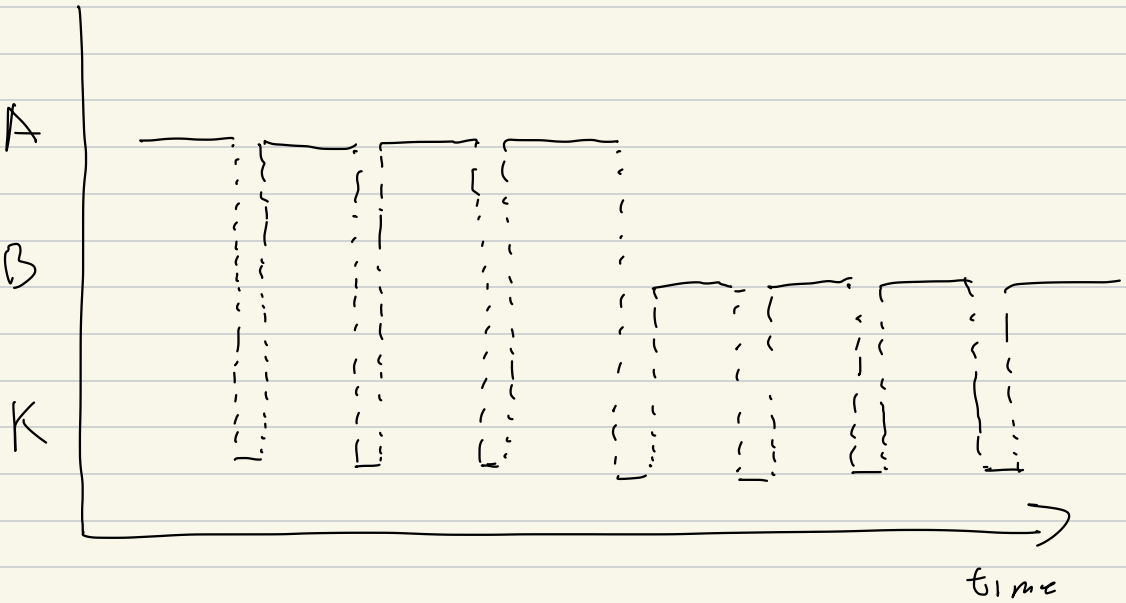
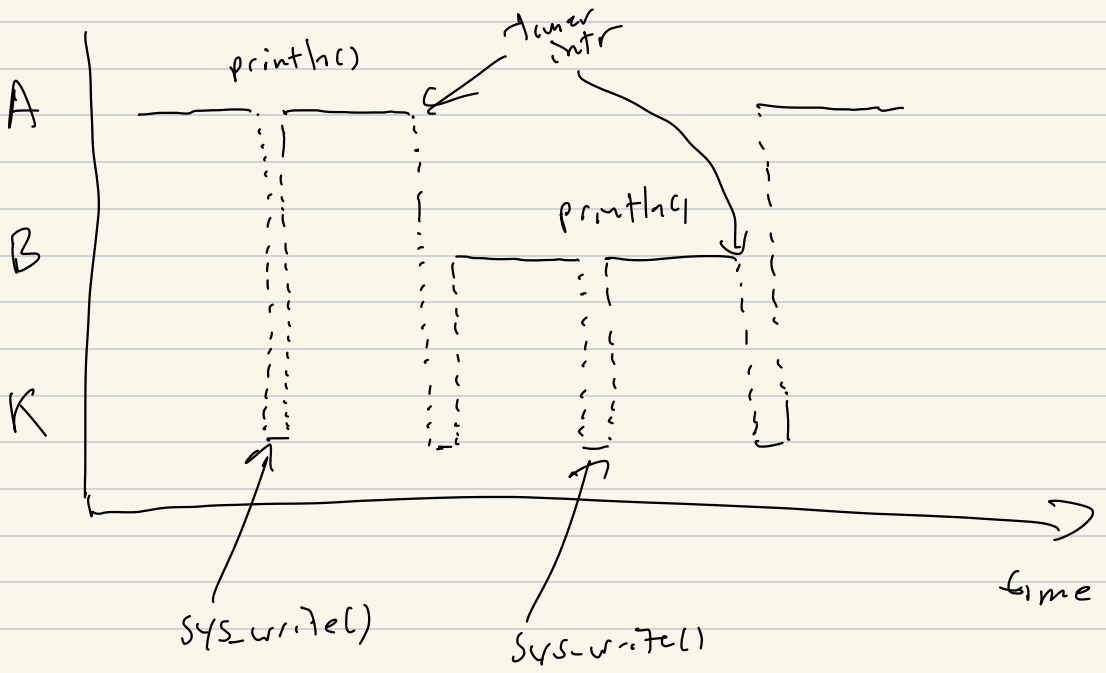
B

CORE<sub>0</sub>



timer interrupt





# Page Tables (Virtual Memory)

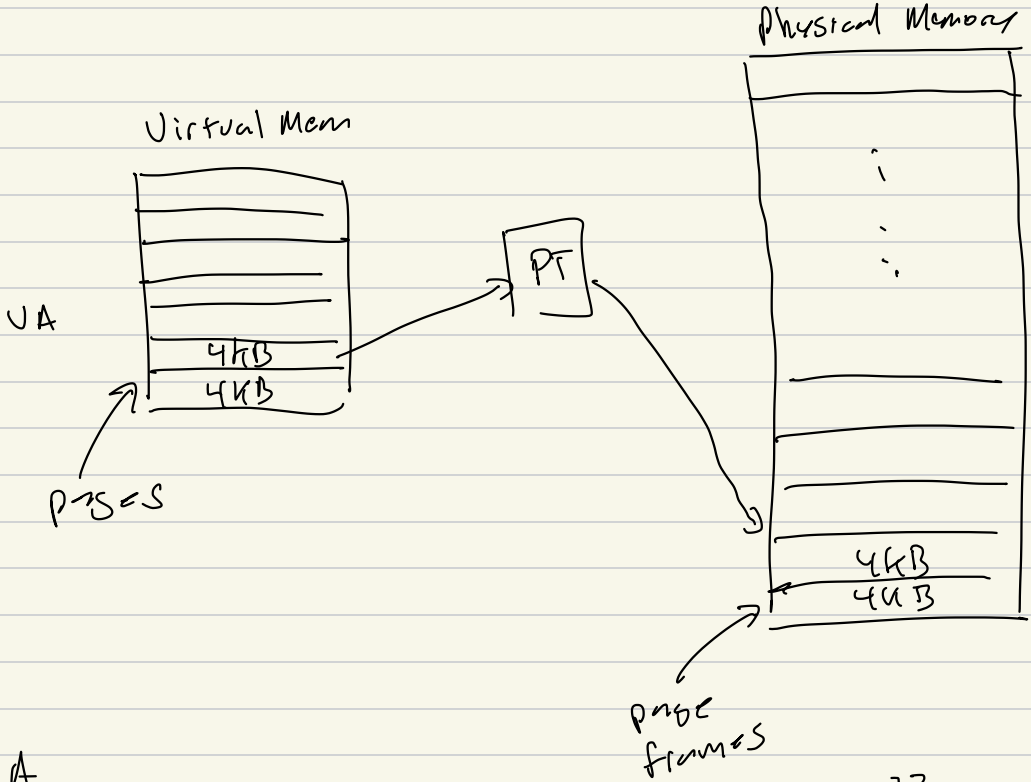
Assume a 32 bit architecture  $2^{32} = 4GB$

Physical Address (PA)

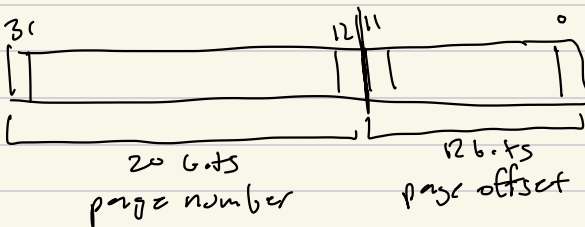
Page size = 4KB

Virtual Address (VA)

$2^{12}$  bytes



VA



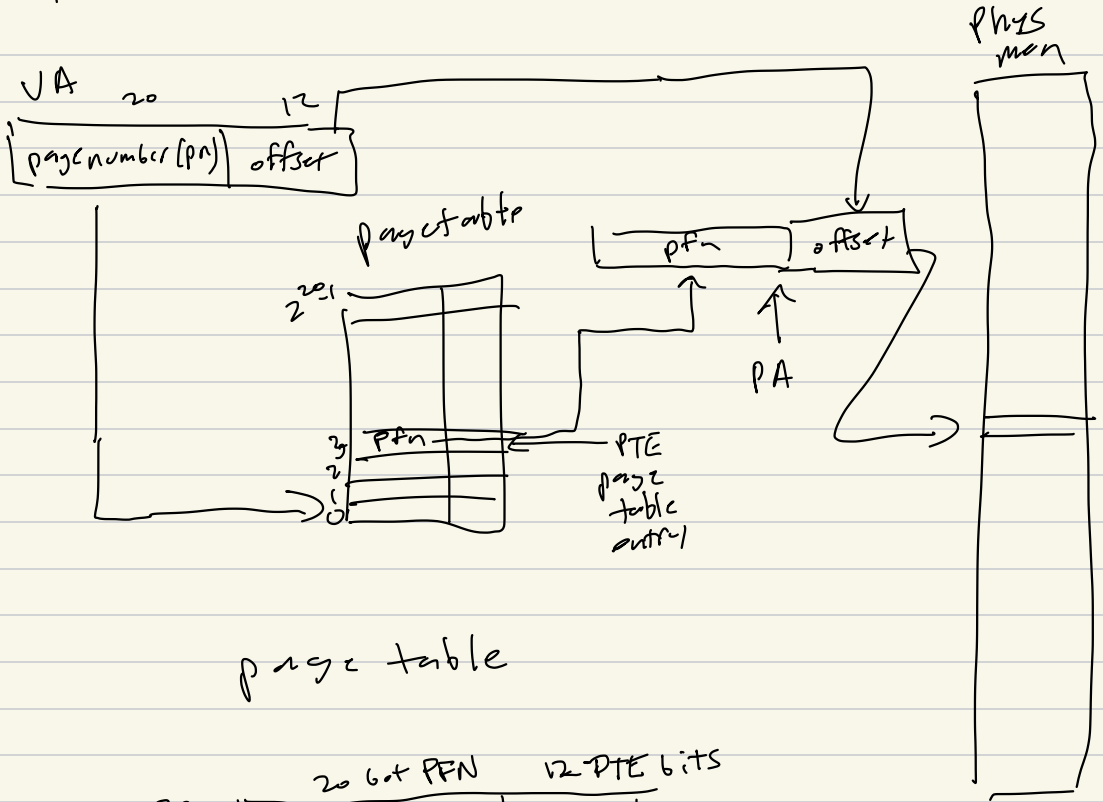
$$2^{32} = 4GB$$

$$\frac{2^{32}}{2^{12}} = 4KB$$

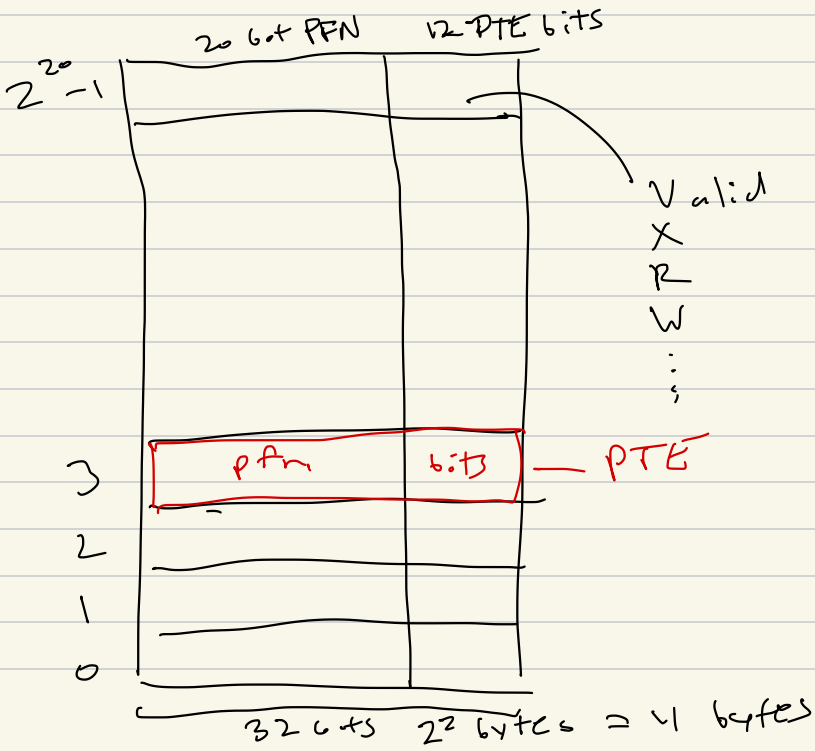
$$= 2^{20} \approx 1 \text{ million} \\ 1 \text{ megabyte}$$

VA  $\rightarrow$  PA

# Translation



## page table



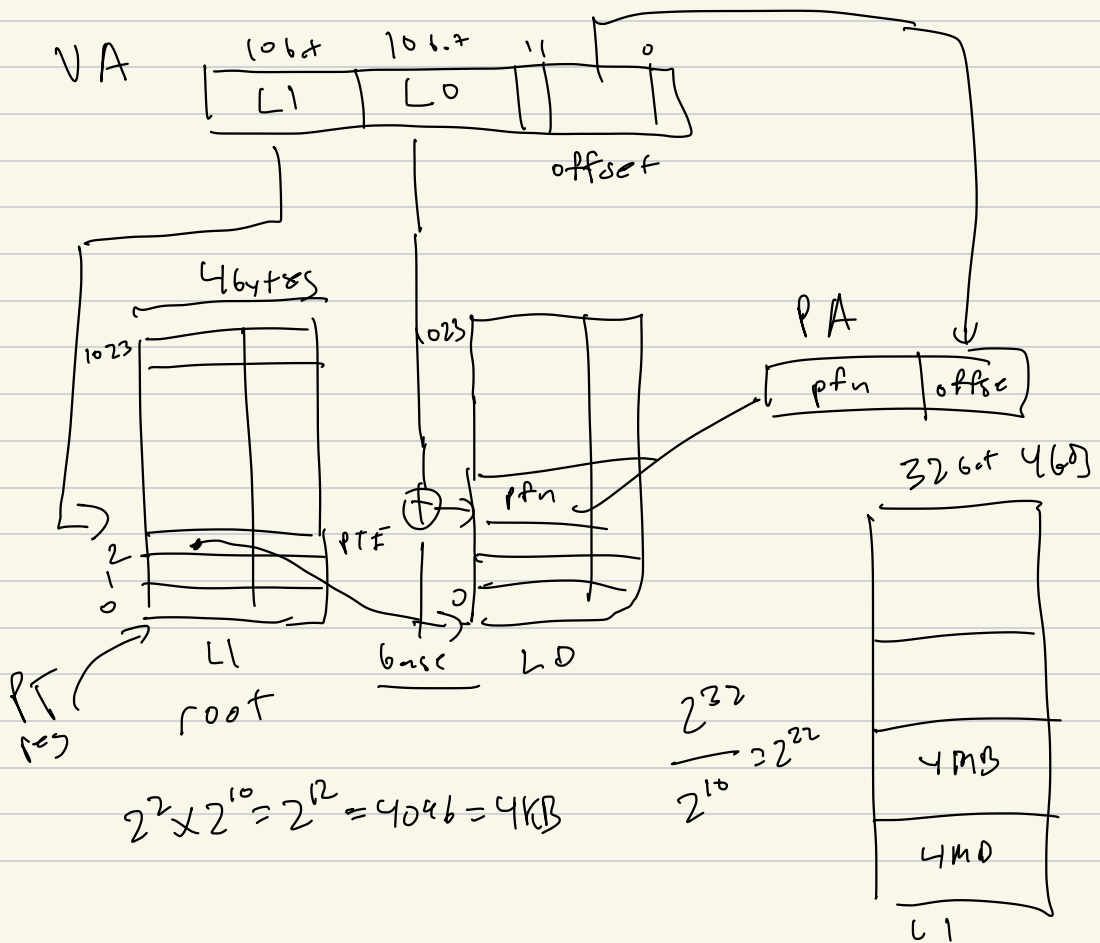
What is the size of the Page Table?

$$2^2 \times 2^{20} = 2^{22} = 4 \text{ MB}$$

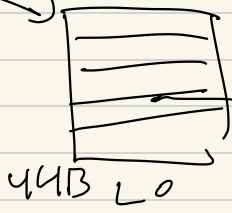
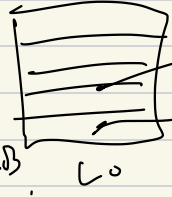
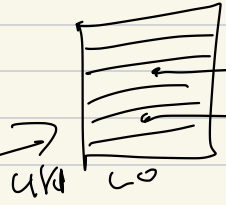
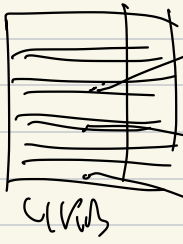
PTE

100 procs  $100 \times 4 \text{ MB} = 400 \text{ MB}$

### Multi-level Page Tables (Sparse)



root(L1)



RAM

